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What is Claimed is:

1. A hot patch system for changing of code in a processor comprising, in combination:

a memory for storing a plurality of instructions;

a program counter coupled to the memory for indexing of the memory to access an instruction; and

a cache system coupled to the memory and to the program counter for comparing information associated with the instruction from memory with information stored in the cache system and for altering an instruction stream when there is a comparison match.

2. A hot patch system in accordance with Claim 1 wherein the cache system comprises:

a cache for storing information;

a register coupled to the cache for storing the information associated with the instruction from memory that is to be compared to the information stored in the cache; and

cache control logic coupled to the cache for controlling insertion of one of the instruction from the memory or an instruction from the cache system into the instruction stream.

3. A hot patch system in accordance with Claim 2 further comprising a switching device coupled to the memory, cache, and the cache control logic for inserting one of the instruction from the memory unit or the instruction from the cache system into the instruction stream.

4. A hot patch system in accordance with Claim 3 wherein the cache comprises a plurality of cache lines wherein each cache line has at least a first field for storing flag information, a second field for storing a cache line instruction, and a third field for storing information which is to be compared with information stored in the register.

5. A hot patch system in accordance with Claim 4 wherein the third field stores a memory address.

6. A hot patch system in accordance with Claim 4 wherein the third field stores an instruction.

7. A hot patch system in accordance with Claim 4 wherein the cache is one of a single direct mapped cache or a single fully associative cache.

8. A hot patch system in accordance with Claim 4 wherein the cache comprises:

an address cache; and

an instruction cache.

9. A hot patch system in accordance with Claim 2 further comprising a mask register coupled to the cache for controlling how information associated with the instruction from the memory is to be compared with information in the cache and for modifying the information in the cache.

10. A hot patch system in accordance with Claim 6 wherein the mask register is a global mask.

11. A hot patch system in accordance with Claim 6 wherein the mask register is a local mask.

12. A hot patch circuit in accordance with Claim 7 wherein the switching device is a multiplexer having a first input coupled to the cache, a second input coupled to the memory, and a third input coupled to the cache control logic.

13. A hot patch circuit in accordance with Claim 5 wherein the switching device comprises:

a first multiplexer having a first input coupled to the address cache, a second input coupled to the instruction cache, and a third input coupled to the cache control logic; and

a second multiplexer having a first input coupled to an output of the first multiplexer, a second input coupled to the memory unit, and a third input coupled to the cache control logic.

14. A hot patch circuit in accordance with Claim 3 further comprising a status buffer having an input coupled to the cache, an input coupled to the switching device and an input coupled to the cache control logic for storing information related to the operation of the circuit.

15. A hot patch circuit in accordance with Claim 8 wherein the cache control logic has priority flags for discriminating priority between an address cache hit and an instruction cache hit.

16. A method of altering the code of a pipeline processor comprising the steps of:

storing a plurality of instructions in memory;

storing information in a cache;

indexing of the memory to access an instruction;

comparing information associated with the instruction from memory with the information in the cache; and

inserting an instruction from the cache into the instruction stream when the information associated with the instruction from memory matches the information in the cache.

17. The method of Claim 16 further comprising the step of inserting the instruction from memory into the instruction stream when the information associated with the instruction from memory does not match the information in the cache.

18. The method of Claim 16 wherein the step of storing information in the cache further comprises the step of programing a plurality of cache lines in the cache to store a first field for storing flag information, a second field for storing a cache line instruction, and a third field for storing information which is to be compared with information stored in the register.

19. The method of Claim 18 wherein the third field is programmed with memory addresses.

20. The method of Claim 18 wherein the third field is programmed with memory instructions.